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Total No. of Questions : 09] [Total No. of Pages : 03

Paper ID [CS201]

MAY - 08

(Please fill this Paper ID in OMR Sheet)

B.Tech. (Sem - 3rd)

COMPUTER ARCHITECTURE (CS - 201)

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

(10 × 2 = 20)

Q1) Choose the correct or best alternative in the following:

a) Which logic is known as universal logic?

(i) PAL logic (ii) NAND logic

(iii) MUX logic (iv) Decoder logic

b) The time for which the D-input of a D-FF must not change after the clock is applied is known as

(i) Hold time. (ii) Set-up time.

(iii) Transition time. (iv) Delay- time.

c) How many memory chips of (128 × 8) are needed to provide a memory capacity of 4096 × 16 ?

(i) 64 (ii) 16

(iii) 32 (iv) None of these

d) In addition of two signed numbers, represented in 2's complement form generates an overflow if

(i) $A \cdot B = 0$ (ii) $A \oplus B = 0$

(iii) $A \oplus B = 1$ (iv) $A + B = 1$

Where **A is** the carry in to the sign bit position and B is the carry out of the **Sign bit** position.

e) Addition of $(1111)_2$ to a 4 bit binary number 'A' results:-

(i) Incrementing A (ii) Addition of $(F)_H$

(iii) No change. (iv) Decrementing A

f) In a microprocessor system, suppose, TRAP, HOLD, RESET Pin got activated at the same time, while the processor was executing some instructions, then it will first respond to

(i) TRAP (ii) HOLD

(iii) RESET (iv) None

g) Pseudo instructions are

(i) Machine instructions. (ii) Logical instructions.

(iii) Micro instructions. (iv) Instructions to assembler.

h) An attempt to access a location not owned by a Program is called

(i) Bus conflict. (ii) Address fault.

(iii) Page fault. (iv) Operating system fault.

i) Briefly write about 8255 chip.

j) Compare SPMD and MIMD machine.

Section - B

(4 × 5 = 20)

Q2) A RAM chip 4096 × 8 bits has two enable lines. How many pins are needed for the integrated circuit Package? Draw a block diagram and label all input and outputs pins of the RAM. What is the main feature of random access memory?

Q3) The RAM IC as described above is used in a microprocessor system, having 16 bit address line and 8-bit data line. It's enable- 1 input is active when A_{15} and A_{14} bits are 0 & 1 and enable-2 input is active when A_{13}, A_{12} bits are 'X' and'O'. What shall be the range of addresses that is being used by the RAM.

Q4) Give the comparison between & examples of hardwired control unit and microprogrammed control unit.

Q5) What do you mean by Fetch cycle, instruction cycle, machine cycle, interrupt acknowledgement cycle.

Q6) Design a CPU that meets the following specifications:
It can access 64 words of memory, each word being 8-bit long. The CPU does this by outputting a 6-bit address on its output pins A[5,.....0] and reading in the 8-bit value from memory on inputs D[7,.. ...0]. It has one 8-bit accumulator, 8-bit address register, 6-bit program counter, 2-bit instruction register, 8-bit data register.
The CPU must realise the following instruction set:

Instruction	Instruction Code	Operation
ADD	00 AAAAAA	AC ← AC +M [AAAAAA]
AND	01 AAAAAA	AC ← AC ^ M [AAAAAA]
JMP	10 AAAAAA	Go to AAAAAA
INC	11 xxxxxx	AC ← AC + 1

Section - C

(2 × 10 = 20)

Q7) (a) What do you mean by software & hardware interrupts? How these are used in a microprocessor system?

(b) What are the reasons of Pipe-Line conflits in a Pipe Lined processor? How are they resolved?

Q8) Draw the block diagram of 8251 and transfer data from CPU to peripheral device at 9600 baud, 2 stop bits, even parity. Store 256 bytes of data at memory location mylocation

Q9) What do you mean by initialisation of DMA controller? How DMA controller works? Explain with suitable block diagram.