

Roll No.

Total No. of Pages : 02

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B.Sc. (CS) (Sem.-2)  
**COMPUTER SYSTEM ARCHITECTURE**

Subject Code : BCS-206

M.Code : 71511

Date of Examination : 18-07-22

Time : 3 Hrs.

Max. Marks : 60

**INSTRUCTIONS TO CANDIDATES :**

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains SIX questions carrying TEN marks each and a student has to attempt any FOUR questions.

**SECTION-A**

1. Answer briefly :

- (a) Stored Program Concept
- (b) Control Unit
- (c) Micro Operations
- (d) Common Bus System
- (e) Instruction Cycle
- (f) RAM and ROM
- (g) USB port
- (h) Memory Hierarchy
- (i) Cache Memory
- (j) Interrupt Initiated I/O.

## SECTION-B

2. Solve the following :

- (a) A hard disk with a transfer rate of 10 Mbytes/ second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?
- (b) Consider a 16-way set associative cache which holds 64 KB of data. The size of physical address is of 40 bits. A cache block consists of 4 words. Every data word is of 32 bits. Assuming that all cache entries are initially empty and data words are word-addressable, find the size of Tag, Set and Offset field in bits.

3. Discuss in detail :

- (a) Harvard Architecture
- (b) Layered Approach Architecture.

4. What is the difference between synchronous and asynchronous data transfer. Discuss in detail about the concept of strobe and handshaking.

5. Explain the Von Neumann Architecture in detail and discuss about its significance.

6. Write a note on the concept of addressing modes and explain each type of addressing mode with examples.

7. What is Flynn's classification? Explain in detail.

**NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.**