Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech. (Electrical & Electronics Engineering / Electrical Engineering)
(Sem.–4)

DIGITAL ELECTRONICS

Subject Code :BTEE-401-18
M.Code :77606
Date of Examination : 02-07-22

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) Realize A'B +AB' using NAND gate.

b) State Duality theorem.

c) Draw 2:4 decoder.

d) What are the advantages of CMOS?

e) Draw 4 bits parallel to serial shift register.

f) What are the disadvantages of weighted register?

g) Give the memory organization.

h) Explain the limitation of K-map.

i) Enlist various counters.

j) Explain BCD codes.

SECTION-B

2. Convert 79 and 56 decimal numbers in other number systems.

3. Draw and explain 32:1 Mux using 2:1 Mux only.

4. Design JK flip flop using SR flip flop.

5. Design voltage to frequency and voltage to time conversion converters.

6. Draw and explain 3 bit up down synchronous counter.

SECTION-C

7. Draw and explain the various types of TTL logic family.

8. Design Binary to Grey code and Grey to binary code converters.

9. Explain the various types of digital to analog converters.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.