Roll No. | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 18

B.Tech. (CSE&DS) (Sem.–4)

# COMPUTER ORGANISATION AND ARCHITECTURE

Subject Code : BTES-401-18

M.Code : 91949

Date of Examination : 11-07-22

Time : 3 Hrs. Max. Marks : 60

**INSTRUCTIONS TO CANDIDATES :**

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

## SECTION-A

**Write briefly :**

1. What do you mean by registers? Explain.
2. Explain in brief about carry save multiplier.
3. Explain in brief about instruction execution cycle.
4. Differentiate between privileged and non-privileged instructions.
5. Explain in brief about Random Access memoiy.
6. Explain in brief about throughput of a pipeline processing.
7. What do you mean software interrupts? Explain.
8. What is the purpose of Parallel Processing?
9. Explain in brief about Memory Interleaving.
10. What are the advantages of cache memory?

## SECTION-B

11. Write a detailed note on RTL interpretation of instructions.
12. Write a detailed note on Direct Memory Access (DMA).
13. Explain in brief about cache coherence problem.
14. Explain in detail about mapping functions.
15. Explain in detail about write policies.

## SECTION-C

16. Write a detailed note on Addressing Modes.
17. Explain in detail about software interrupts and exceptions.
18. Write a detailed note on Pipeline Hazards.



**NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student**.