Roll No. | | | | | | | | | | |

Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Date of Examination : 17-01-23

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

1. **Write briefly :**

a) Draw symbol and construct truth table for three inputs NAND gate.

b) Which gates are called universal gates and why?

c) Which is the fastest ADC and why?

d) The t_{pd} for each flip flop is 30 ns determine the maximum operating frequency of MOD- 32 ripple counter.

e) What are magnitude comparators?

f) Compare PLA and PAL.

g) What is race around condition and how it is removed?

h) Compare Asynchronous counter and synchronous counter.

i) What do you mean by dataflow in VHDL?

j) Define propagation delay time and figure of merit.

SECTION-B

2. Implement EX-OR gate using only NAND gates.

3. What is half adder? Write its truth table and develop its logic circuit.

4. Implement the following function using all 4:1 multiplexers.

   $f(A, B, C, D, E) = \sum m (0, 1, 2, 3, 6, 8, 9, 10, 13, 15, 17, 20, 24)$

5. Explain the working of R-2R Ladder type DAC with a suitable circuit.

6. What do you mean by data types and objectives in VHDL?

SECTION-C

7. Simplify $F (W, X, Y, Z) = \Pi (1, 3, 7, 10, 13) + d (0, 2, 4, 5)$ using K-Map. Realize the simplified expression in SOP and POS.

8. Implement a BCD to seven segment decoder using a 4 line to 16 line decoder.

9. Design a Mod 6 up down counter.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.