Roll No. | | | | | | | | | | |

Total No. of Pages : 02

Total No. of Questions : 09

B.Tech. (IT) (Sem.–3)

# COMPUTER ARCHITECTURE

Subject Code : BTES-302-18

M.Code : 76394

Date of Examination : 21-01-2023

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

## SECTION-A

1. **Answer briefly :**

a) What are the advantages of carry look-ahead adder?

b) What do you mean by input-output subsystems?

c) Explain in brief about non-restoring Division.

d) What do you mean by privileged instructions? Explain.

e) What do you mean by DMA? Explain.

f) Explain in brief about the throughput of a pipeline processing.

g) What do you mean by parallel processing? Also, write the advantages of parallel processing.

h) What do you mean by Pipeline Hazards? Explain.

i) What do you mean by Cache Misses? Explain.

j) What are two main cache write policies?



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## SECTION-B

2. Write a detailed note on Booth Multiplier.

3. Differentiate between hardwired and micro-programmed CPU control unit design.

4. Explain about arithmetic pipelining with an example.

5. Explain in detail about Control Hazards.

6. Write a detailed note on write policies.

## SECTION-C

7. Explain in detail about following :

   a) Carry save multiplier

   b) Shift and add multiplier.

8. Explain in detail about I/O device interfaces.

9. Explain the following terms in detail :

   a) Cache Coherency

   b) Memory Interleaving.

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