Roll No. | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech. (Artificial Intelligence (AI) and Data Science / CSE / (CSE)(AI&ML) /(CSE)(Data Science) /(CSE)(IOT)/(Data Science)/ IT / CSE (Internet of Things and Cyber Security including Block Chain Technology)) (Sem.–3)

DIGITAL ELECTRONICS

Subject Code : BTES301-18

M.Code : 76435

Date of Examination : 24-05-2023

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) What is the need of digital electronics? Discuss.

b) List the various disadvantages of Boolean algebra.

c) Differentiate between combinational and sequential circuits.

d) What is the need of a flip flop? Discuss.

e) What do you mean by MUX? Discuss.

f) What do you mean by excitation table? Discuss.

g) What do you mean by race around condition? Discuss.

h) Discuss the significance of D flip-flop.

i) Write down the need of sample and hold circuit.

j) What do you mean by memory cycle? Discuss.

SECTION-B

2. Implement the half adder using :

   a) AOI

   b) NAND gates only .

3. In an industry four operations Temperature, Pressure, Level and Humidity are to be encoded. Design a priority encoder in which Temperature must have the highest priority then Pressure followed by Level and Humidity is having the lowest priority.

4. Explain the working of a JK flip-flop. Also, discuss how the problem of SR flip flop is solved in JK flip flop?

5. Draw the diagram and discuss the working of R-2R type D/A converter in detail.

6. Explain the ROM organization and its comparison with RAM.

SECTION-C

7. Draw and explain the working of Successive approximation and dual slope A/D converters.

8. a) Reduce the following expression to simplest form using K map method F(A,B,C,D) = $\sum m$ (0,2,5,6,7,10,11,12)

   b) Draw the logical diagram and explain the working of BCD adder.

9. Explain :

   a) FPGA

   b) Gray and Excess 3 codes

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.