Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(ECE) (Sem–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Date of Examination : 05-06-2023

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) Design NOR gate using universal gates.

b) Minimize using Boolean algebra $x'yz + yz' + x$.

c) Discuss VHDL constructs.

d) Convert $(1011110)_{Binary}$ to Gray code.

e) Multiply 101101 by 1001.

f) Convert $(1001\ 1000)_{BCD}$ to Excess-3 code.

g) Implement 4:1 multiplexer using 2:1 multiplexers.

h) Convert the following expressions to canonical POS : (A'+B+C) (B'+C').

i) Write De-Morgan's theorem.

j) Design Half Subtractor circuit.

SECTION-B

2. Implement the following function using Decoder

   $F(A,B,C,D) = \sum m(0,1,2,3,6,7,8,12)$.

3. Design BCD to 7 Segment Display.

4. How Master slave flip flop is used to avoid race around condition.

5. Write short note on PAL, PLA, CPLD.

6. Discuss various modeling styles in VHDL.

SECTION-C

7. Describe the various characteristics of D/A convertor. Also, explain the working of R–2R D/A convertor.

8. Design MOD 7 counter using JK flip flop.

9. Minimize using K Map technique :

   $F(w,x,y,z) = \sum m\,(0,1,2,3,5,7,8,12,13,14,15) + d(4,11)$

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.