Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Date of Examination: 12-12-2023

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) Why NAND and NOR are called universal gates?

b) Minimize using Boolean algebra AB'C'D + AC + BC'D + D.

c) Define propagation delay in logic families.

d) Implement 4:1 multiplexer using 2:1 multiplexer.

e) Convert the following expressions to canonical SOP: A'B'C+BC

f) Prove that AB+A'C+BC = AB+A'C.

g) Discuss PAL and PLA circuits.

h) Why priority encoders are preferred?

i) Discuss the working of BCD adder circuit.

j) Convert $(0010\ 0110)_{BCD}$ to Excess-3 code.

SECTION-B

2. Differentiate between CPLD and FPGA.

3. Name various modelling styles in VHDL, give example of Structural style of modelling.

4. Describe the working of 2:4 decoder. Can decoder be used as a demultiplexer?

5. Design 2bit magnitude comparator.

6. Define Race Around Condition. How Master slave flip flop is used to avoid Race Around Condition?

SECTION-C

7. Minimize using K Map technique

   $F(w,x,y,z) = \Sigma m\ (0,1,2,7,9,11,14,15) + d(3,5,12,13)$.

8. Describe various characteristics of D/A converter. Also, explain the working of weighted resistor D/A convertor.

9. Design Binary to Gray code convertor.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.