Roll No. | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Date of Examination : 13-06-2024

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

(a) What are SOP & POS forms?

(b) Explain barrel shifter.

(c) Define serial and parallel adders.

(d) Give excitation table of SR, JK, D & T flip flops.

(e) What is pseudo random binary sequence generator?

(f) Draw SISO, SIPO shift registers.

(g) What do you mean by propagation delay?

(h) Explain fan-in and fan-out.

(i) What are the various advantages of VHDL modeling?

(j) Enlist various objects of VHDL.

SECTION-B

2. Design BCD adder.

3. Design 2 bit up-down synchronous counter.

4. Draw and explain CMOS logic family.

5. Write a program of full adder using dataflow style modeling in VHDL.

6. Explain weighted resistor converter.

SECTION-C

7. Design BCD to seven segment code converter.

8. Design clocked SR and JK flip flops and explain their working.

9. Draw and explain PAL and PLA circuits.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.