Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(AI&ML/ DS/CSE/IT/(Internet of Things and Cyber Security including Block Chain Technology) (Sem.–3)

DIGITAL ELECTRONICS

Subject Code : BTES301/18

M.Code : 76435

Date of Examination : 28-05-2024

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Write briefly :**

   a. What is the need of Digital Electronics? Discuss.

   b. State and prove DeMorgan's theorems.

   c. Compare combinational and sequential circuits.

   d. Draw the symbol of Exclusive-NOR gate and write down its truth table.

   e. What do you mean by donot care condition? What is its importance?

   f. Discuss the significance of FPGA.

   g. List the advantages and disadvantages of Digital Signals.

   h. What do you mean by memory cycle? Discuss.

   i. Write down the advantages and disadvantages of dual slope A/D converter.

   j. What do you mean by MOD of a counter? How many flip-flops are required for MOD-10 counter?

SECTION-B

2. Convert the 324.25 decimal number to equivalent binary, hexadecimal and octal numbers.

3. Reduce the following expression to simplest forms using Karnaugh map minimization

   F(A, B, C, D) = $\sum m$ (l,3,5,11,12,13) + d (0,14) where d stands for Don't care.

4. Discuss the need of memory. Differentiate between PROM, EPROM, EEPROM and RAM.

5. Discuss the working of a master slave J K flip-flop. Write down its advantages and disadvantages also.

6. How R-2R type D/A converter is different from weighted type D/A converter? Explain its working in detail.

SECTION-C

7. Explain in detail the working of Counter type and successive approximation A/D converters. Also mention their advantages and disadvantages.

8. Discuss :

   a) BCD to 7 segment decoder

   b) Programmable logic array.

9. Design a 4 bit synchronous counter having the following states

   0000, 0001, 0010, 0011, 0100, 0101, 0110, 0000, 0001……

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.