Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech. (IT) (Sem.–3)

COMPUTER ARCHITECTURE

Subject Code : BTES-302-18

M.Code : 76394

Date of Examination : 19-06-2024

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a) What is an instruction format in computer architecture?

b) What is control unit?

c) Explain the concept of virtual memory.

d) Difference between arithmetic shift left and arithmetic shift right.

e) USB.

f) Pipelining.

g) Cache memory.

h) What are the registers? Can they be called memory?

i) Discuss look-ahead adder

j) Compare RISC and CISC.

SECTION-B

2. Explain all the phases of instructions cycle.

3. What is DMA? Give an example where DMA mode of data transfer is used?

4. What is pipeline control? Explain.

5. What is multilevel memory system? Explain with the help of a diagram.

6. How the data is represented in computer architecture? Explain with an example.

SECTION-C

7. What are the addressing modes? Explain the various addressing modes with suitable examples.

8. What is the need of replacement algorithms in memory organization? Explain with examples.

9. Explain various mechanisms of data transfer from peripheral devices.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.