Roll No. | | | | | | | | | | | | |

Total No. of Questions : 09

Total No. of Pages : 02

B.Tech. (ECE/ME) (Sem–7,8)

COMPUTER ORGANISATION AND ARCHITECTURE

Subject Code : BTES-401-18

M.Code : 90491

Date of Examination : 24-04-2024

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

1. Write short note on the following :

a) What is Control Unit?

b) Discuss carry look-ahead adder.

c) Write functioning of USB.

d) Define concept of Memory Organization.

e) What is meant by division restoration?

f) Write use of software interrupts.

g) What are CPU registers?

h) Discuss floating point arithmetic.

i) Briefly explain cache size.

j) List advantages of pipelining.

(S2)-5

SECTION-B

2. Explain different addressing modes used in central processing unit.

3. What are the advantages and disadvantages of hardwired and micro-programmed design approaches?

4. What is DMA? Give an example where DMA mode of data transfer is useful.

5. Discuss the role of cache coherency in parallel processors.

6. How the data is represented in computer architecture? Explain with example.

SECTION-C

7. Briefly explain the block diagram and instruction set of 8085 processor.

8. What is the need of replacement algorithms in memory organization? Explain with example.

9. Discuss the role of Pipelining for data processing in computer organization. How it increases the throughput?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.