

Roll No.

Total No. of Pages : 02

Total No. of Questions : 09

B.Tech. (ECE)(Sem.-3)
DIGITAL CIRCUIT AND LOGIC DESIGN

Subject Code :BTEC-302

M.Code : 96261

Date of Examination : 11-12-2025

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

1. Write briefly :

- a) Convert Binary number 11101.1 into Decimal, Octal and Hexadecimal number systems.
- b) Explain ASCII codes.
- c) What is Complement law in Boolean algebra?
- d) Design $A'B' + AB$ using NAND and NOR gates only.
- e) Draw 2:4 decoder.
- f) What are the limitations of K-Map?
- g) Give the expression for select lines in Multiplexer.
- h) Define shift registers.
- i) What do you mean by accuracy in A/D converters?
- j) Give memory organization chart.

SECTION - B

2. Subtract 34 from 56 using 2's complement.
3. Minimize $F = \Pi M (0,1,2,3,4,6,7,9,10,11)$ using K Map.
4. Design 2bit Magnitude comparator.
5. Draw and explain SR and JK flip flops.
6. Design Single slope A/D converter.

SECTION - C

7. Classify different types of memories.
8. Draw and explain DTL logic family circuit diagram.
9. Design universal shift register.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.